

What is claimed:

1        1. A semiconductor device to be used for a CMOS inverter circuit, the  
2        semiconductor device comprising:  
3              a dielectric film formed on a semiconductor substrate;  
4              a SOI film comprising single crystal Si formed on the dielectric layer film;  
5              a gate dielectric film formed on the SOI film;  
6              a gate electrode formed on the gate dielectric film; and  
7              a diffusion layer for source/drain regions formed in source/drain regions of the SOI  
8        film,  
9              wherein, when a power supply voltage of 0.6 V is used,  
10             a thickness of the SOI film is 0.084  $\mu\text{m}$  or greater and 0.094  $\mu\text{m}$  or smaller, and an  
11             impurity concentration of the SOI film is  $7.95 \times 10^{17}/\text{cm}^3$  or greater and  $8.05 \times 10^{17}/\text{cm}^3$  or  
12             smaller.

1        2. A semiconductor device to be used for a CMOS inverter circuit, the  
2        semiconductor device comprising:  
3              a dielectric film formed on a semiconductor substrate;  
4              a SOI film comprising single crystal Si formed on the dielectric layer film;  
5              a gate dielectric film formed on the SOI film;  
6              a gate electrode formed on the gate dielectric film; and  
7              a diffusion layer for source/drain regions formed in source/drain regions of the SOI  
8        film,  
9              wherein, when a power supply voltage of 0.6 V is used,  
10             a thickness of the SOI film is 0.089  $\mu\text{m}$  or greater and 0.099  $\mu\text{m}$  or smaller, and an  
11             impurity concentration of the SOI film is  $8.95 \times 10^{17}/\text{cm}^3$  or greater and  $9.05 \times 10^{17}/\text{cm}^3$  or  
12             smaller.

1           3. A semiconductor device to be used for a CMOS inverter circuit, the  
2 semiconductor device comprising:  
3           a dielectric film formed on a semiconductor substrate;  
4           a SOI film comprising single crystal Si formed on the dielectric layer film;  
5           a gate dielectric film formed on the SOI film;  
6           a gate electrode formed on the gate dielectric film; and  
7           a diffusion layer for source/drain regions formed in source/drain regions of the SOI  
8 film,  
9           wherein, when a power supply voltage of 0.6 V is used,  
10          a thickness of the SOI film is 0.093  $\mu\text{m}$  or greater and 0.103  $\mu\text{m}$  or smaller, and an  
11          impurity concentration of the SOI film is  $0.095 \times 10^{18}/\text{cm}^3$  or greater and  $1.005 \times 10^{18}/\text{cm}^3$   
12          or smaller.

1           4. A semiconductor device to be used for a CMOS inverter circuit, the  
2 semiconductor device comprising:  
3           a dielectric film formed on a semiconductor substrate;  
4           a SOI film comprising single crystal Si formed on the dielectric layer film;  
5           a gate dielectric film formed on the SOI film;  
6           a gate electrode formed on the gate dielectric film; and  
7           a diffusion layer for source/drain regions formed in source/drain regions of the SOI  
8 film,  
9           wherein, when a power supply voltage of 0.6 V is used,  
10          a thickness of the SOI film is 0.096  $\mu\text{m}$  or greater and 0.106  $\mu\text{m}$  or smaller, and an  
11          impurity concentration of the SOI film is  $1.095 \times 10^{18}/\text{cm}^3$  or greater and  $1.105 \times 10^{18}/\text{cm}^3$   
12          or smaller.

1           5. A semiconductor device to be used for a CMOS inverter circuit, the  
2 semiconductor device comprising:  
3           a dielectric film formed on a semiconductor substrate;  
4           a SOI film comprising single crystal Si formed on the dielectric layer film;  
5           a gate dielectric film formed on the SOI film;  
6           a gate electrode formed on the gate dielectric film; and  
7           a diffusion layer for source/drain regions formed in source/drain regions of the SOI  
8 film,  
9           wherein, when a power supply voltage of 0.6 V is used,  
10          a thickness of the SOI film is 0.100  $\mu\text{m}$  or greater and 0.110  $\mu\text{m}$  or smaller, and an  
11          impurity concentration of the SOI film is  $1.195 \times 10^{18}/\text{cm}^3$  or greater and  $1.205 \times 10^{18}/\text{cm}^3$   
12          or smaller.

1           6. A semiconductor device to be used for a CMOS inverter circuit, the  
2 semiconductor device comprising:  
3           a dielectric film formed on a semiconductor substrate;  
4           a SOI film comprising single crystal Si formed on the dielectric layer film;  
5           a gate dielectric film formed on the SOI film;  
6           a gate electrode formed on the gate dielectric film; and  
7           a diffusion layer for source/drain regions formed in source/drain regions of the SOI  
8 film,  
9           wherein, when a power supply voltage of 0.8 V is used,  
10          a thickness of the SOI film is 0.068  $\mu\text{m}$  or greater and 0.078  $\mu\text{m}$  or smaller, and an  
11          impurity concentration of the SOI film is  $7.95 \times 10^{17}/\text{cm}^3$  or greater and  $8.05 \times 10^{17}/\text{cm}^3$  or  
12          smaller.

1           7. A semiconductor device to be used for a CMOS inverter circuit, the  
2 semiconductor device comprising:  
3           a dielectric film formed on a semiconductor substrate;  
4           a SOI film comprising single crystal Si formed on the dielectric layer film;  
5           a gate dielectric film formed on the SOI film;  
6           a gate electrode formed on the gate dielectric film; and  
7           a diffusion layer for source/drain regions formed in source/drain regions of the SOI  
8 film,

9           wherein, when a power supply voltage of 0.8 V is used,  
10          a thickness of the SOI film is 0.074  $\mu\text{m}$  or greater and 0.084  $\mu\text{m}$  or smaller, and an  
11          impurity concentration of the SOI film is  $8.95 \times 10^{17}/\text{cm}^3$  or greater and  $9.05 \times 10^{17}/\text{cm}^3$  or  
12          smaller.

1           8. A semiconductor device to be used for a CMOS inverter circuit, the  
2 semiconductor device comprising:  
3           a dielectric film formed on a semiconductor substrate;  
4           a SOI film comprising single crystal Si formed on the dielectric layer film;  
5           a gate dielectric film formed on the SOI film;  
6           a gate electrode formed on the gate dielectric film; and  
7           a diffusion layer for source/drain regions formed in source/drain regions of the SOI  
8 film,

9           wherein, when a power supply voltage of 0.8 V is used,  
10          a thickness of the SOI film is 0.078  $\mu\text{m}$  or greater and 0.088  $\mu\text{m}$  or smaller, and an  
11          impurity concentration of the SOI film is  $0.095 \times 10^{18}/\text{cm}^3$  or greater and  $1.005 \times 10^{18}/\text{cm}^3$   
12          or smaller.

1           9. A semiconductor device to be used for a CMOS inverter circuit, the  
2 semiconductor device comprising:  
3           a dielectric film formed on a semiconductor substrate;  
4           a SOI film comprising single crystal Si formed on the dielectric layer film;  
5           a gate dielectric film formed on the SOI film;  
6           a gate electrode formed on the gate dielectric film; and  
7           a diffusion layer for source/drain regions formed in source/drain regions of the SOI  
8 film,  
9           wherein, when a power supply voltage of 0.8 V is used,  
10          a thickness of the SOI film is 0.083  $\mu\text{m}$  or greater and 0.093  $\mu\text{m}$  or smaller, and an  
11 impurity concentration of the SOI film is  $1.095 \times 10^{18}/\text{cm}^3$  or greater and  $1.105 \times 10^{18}/\text{cm}^3$   
12 or smaller.

1           10. A semiconductor device to be used for a CMOS inverter circuit, the  
2 semiconductor device comprising:  
3           a dielectric film formed on a semiconductor substrate;  
4           a SOI film comprising single crystal Si formed on the dielectric layer film;  
5           a gate dielectric film formed on the SOI film;  
6           a gate electrode formed on the gate dielectric film; and  
7           a diffusion layer for source/drain regions formed in source/drain regions of the SOI  
8 film,  
9           wherein, when a power supply voltage of 0.8 V is used,  
10          a thickness of the SOI film is 0.087  $\mu\text{m}$  or greater and 0.097  $\mu\text{m}$  or smaller, and an  
11 impurity concentration of the SOI film is  $1.195 \times 10^{18}/\text{cm}^3$  or greater and  $1.205 \times 10^{18}/\text{cm}^3$   
12 or smaller.

1           11. A semiconductor device to be used for a CMOS inverter circuit, the  
2 semiconductor device comprising:  
3           a dielectric film formed on a semiconductor substrate;  
4           a SOI film comprising single crystal Si formed on the dielectric layer film;  
5           a gate dielectric film formed on the SOI film;  
6           a gate electrode formed on the gate dielectric film; and  
7           a diffusion layer for source/drain regions formed in source/drain regions of the SOI  
8 film,  
9           wherein, when a power supply voltage of 1.0 V is used,  
10          a thickness of the SOI film is 0.057  $\mu\text{m}$  or greater and 0.067  $\mu\text{m}$  or smaller, and an  
11 impurity concentration of the SOI film is  $7.95 \times 10^{17}/\text{cm}^3$  or greater and  $8.05 \times 10^{17}/\text{cm}^3$  or  
12 smaller.

1           12. A semiconductor device to be used for a CMOS inverter circuit, the  
2 semiconductor device comprising:  
3           a dielectric film formed on a semiconductor substrate;  
4           a SOI film comprising single crystal Si formed on the dielectric layer film;  
5           a gate dielectric film formed on the SOI film;  
6           a gate electrode formed on the gate dielectric film; and  
7           a diffusion layer for source/drain regions formed in source/drain regions of the SOI  
8 film,  
9           wherein, when a power supply voltage of 1.0 V is used,  
10          a thickness of the SOI film is 0.063  $\mu\text{m}$  or greater and 0.073  $\mu\text{m}$  or smaller, and an  
11 impurity concentration of the SOI film is  $8.95 \times 10^{17}/\text{cm}^3$  or greater and  $9.05 \times 10^{17}/\text{cm}^3$  or  
12 smaller.

1           13. A semiconductor device to be used for a CMOS inverter circuit, the  
2 semiconductor device comprising:  
3           a dielectric film formed on a semiconductor substrate;  
4           a SOI film comprising single crystal Si formed on the dielectric layer film;  
5           a gate dielectric film formed on the SOI film;  
6           a gate electrode formed on the gate dielectric film; and  
7           a diffusion layer for source/drain regions formed in source/drain regions of the SOI  
8 film,  
9           wherein, when a power supply voltage of 1.0 V is used,  
10          a thickness of the SOI film is 0.068  $\mu\text{m}$  or greater and 0.078  $\mu\text{m}$  or smaller, and an  
11 impurity concentration of the SOI film is  $0.095 \times 10^{18}/\text{cm}^3$  or greater and  $1.005 \times 10^{18}/\text{cm}^3$   
12 or smaller.

1           14. A semiconductor device to be used for a CMOS inverter circuit, the  
2 semiconductor device comprising:  
3           a dielectric film formed on a semiconductor substrate;  
4           a SOI film comprising single crystal Si formed on the dielectric layer film;  
5           a gate dielectric film formed on the SOI film;  
6           a gate electrode formed on the gate dielectric film; and  
7           a diffusion layer for source/drain regions formed in source/drain regions of the SOI  
8 film,  
9           wherein, when a power supply voltage of 1.0 V is used,  
10          a thickness of the SOI film is 0.072  $\mu\text{m}$  or greater and 0.082  $\mu\text{m}$  or smaller, and an  
11 impurity concentration of the SOI film is  $1.095 \times 10^{18}/\text{cm}^3$  or greater and  $1.105 \times 10^{18}/\text{cm}^3$   
12 or smaller.

1           15. A semiconductor device to be used for a CMOS inverter circuit, the  
2 semiconductor device comprising:  
3           a dielectric film formed on a semiconductor substrate;  
4           a SOI film comprising single crystal Si formed on the dielectric layer film;  
5           a gate dielectric film formed on the SOI film;  
6           a gate electrode formed on the gate dielectric film; and  
7           a diffusion layer for source/drain regions formed in source/drain regions of the SOI  
8       film,  
9           wherein, when a power supply voltage of 1.0 V is used,  
10          a thickness of the SOI film is 0.076  $\mu\text{m}$  or greater and 0.086  $\mu\text{m}$  or smaller, and an  
11          impurity concentration of the SOI film is  $1.195 \times 10^{18}/\text{cm}^3$  or greater and  $1.205 \times 10^{18}/\text{cm}^3$   
12          or smaller.

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